during periods of data access activity, said power supplied during periods of no data access activity being less than said power supplied during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

14. (Amended) The dynamic power management device of Claim 4, wherein said power control means comprises a pulse width modulator circuit, [responsive to] said logic control means [for generating] causing said pulse width modulator circuit to generate a pulse width modulated signal having pulses with pulse widths proportional to said specified voltage output.

16. (Amended) The dynamic power management device of Claim 15, wherein said power control means further comprises a FET driver circuit coupled to said pulse width modulator circuit, said FET driver circuit generating a variable voltage having a voltage level proportional to the pulse widths of pulses in [response to] said filtered pulse width modulated signal.

21. (Amended) An integrated circuit for controlling the power supplied to a solid state memory integrated circuit having a first operation period for maintaining information stored in said memory integrated circuit, a second operation period for refreshing data stored in said memory integrated circuit, and a third operation period for accessing said memory integrated circuit, said memory integrated circuit having a first voltage requirement during said first operational period, a second voltage requirement during said second operational period and a third voltage requirement during said third operational period, said integrated circuit comprising:

power control means for supplying a variable voltage

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

to said memory integrated circuit; and

logic control means for causing said power control means to supply to said memory integrated circuit a first voltage during said first operation period, a second voltage different from said first voltage during said second operation period, and a third voltage different from said first and second [voltage] voltages during said third operation period.

23. (Amended) A dynamic power management device for supplying power to a solid state memory integrated circuit in a computer system having a power source [providing] supplying a substantially constant voltage, said dynamic power management device comprising:

power control means coupled to said power source for supplying a variable voltage to said memory integrated circuit, said variable voltage being less than or equal to said substantially constant voltage [provided] supplied by said power source; and

logic control means for generating address and control signals for said memory integrated circuit and for controlling said power control means to supply power to said memory integrated circuit at a level to maintain memory information in said memory integrated circuit during periods of no data access activity and to supply power at a level to [exchange] read and write memory information [with] in said memory integrated circuit during periods of data access activity, said power supplied during periods of no data access activity being less than said power supplied during periods of data access activity, whereby power consumption of said memory integrated circuit is curtailed.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233